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1 **A CMOS Miller hold capacitance sample-and-hold circuit to reduce cl sharing effect and clock feedthrough**
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ASIC/SOC Conference, 2002. 15th Annual IEEE International , 25-28 Sept. 20
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2 **Stray-insensitive sample-delay-hold buffers for high-frequency switched-capacitor filters**
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13 **A single-power-supply 10-b video BiCMOS sample-and-hold IC**
Tsugaru, K.; Sugimoto, Y.; Noda, M.; Ito, T.; Suwa, Y.;
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14 **A 12-bit, 1-MHz, two-step flash ADC**
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15 **Development of a switched capacitor based multi-channel transient waveform recording integrated circuit**
Kleinfelder, S.A.;
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Lapoe Lynn, Paul Ferguson

August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

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2 Leakage current cancellation technique for low power switched-capacitor circuits

Louis S. Y. Wong, Shohan Hossain, Andre Walker

August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

Full text available: pdf(443.09 KB) Additional Information: full citation, references, citings, index terms

Keywords: amplifier, analog, leakage current, low power, sample and hold, switched-capacitor circuit

3 Behavioral simulation for noise in mixed-mode sampled-data systems

Edward W. Y. Liu, Alberto L. Sangiovanni-Vincentelli

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(514.16 KB) Additional Information: full citation, references, citings, index terms

4 High speed converters, amplifiers, and low power analog circuits: A low-power design methodology for high-resolution pipelined analog-to-digital converters

Reza Lotfi, Mohammad Taherzadeh-Sani, M. Yaser Azizi, Omid Shoaei

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(269.36 KB) Additional Information: full citation, abstract, references, index terms

In this paper a general method to design a pipelined ADC with minimum power consumption is presented. By expressing the total static power consumption and the total

input-referred noise of the converter as functions of the capacitor values and the resolutions of the converter stages, a simple optimization algorithm is employed to calculate the optimum values of these parameters, which lead to minimum power consumption while a specified noise requirement is satisfied. To determine the bias curren ...

Keywords: low-power design, operational amplifiers, pipelined analog-to-digital converters

5 Simulation methods for RF integrated circuits

Ken Kundert

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(97.56 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

The principles employed in the development of modern RF simulators are introduced and the various techniques currently in use, or expected to be in use in the next few years, are surveyed. Frequency and time domain techniques are presented and contrasted, as are steady state and envelope techniques and large and small signal techniques.

Keywords: RF integrated circuits, envelope techniques, integrated circuit modelling, modern RF simulators, simulation methods, small signal techniques, state techniques, time domain techniques

6 Micro power "relative precision" 13 bits cyclic RSD A/D converter

A. Heubi, P. Balsiger, F. Pellandini

August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**

Full text available: pdf(93.99 KB) Additional Information: full citation, references, citings, index terms

7 A prototype framework for knowledge-based analog circuit synthesis

R. Harjani, R. A. Rutenbar, L. R. Carley

June 1988 **Papers on Twenty-five years of electronic design automation**

Full text available: pdf(1.06 MB) Additional Information: full citation, references, index terms

8 A prototype framework for knowledge-based analog circuit synthesis

R. Harjani, R. A. Rutenbar, L. R. Carley

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings, index terms

An organization for a knowledge-based analog circuit synthesis tool is described. Analog circuit topologies are represented as a hierarchy of functional blocks; a planning mechanism is introduced to translate performance specifications between levels in this circuit hierarchy. A prototype implementation, OASYS, synthesizes sized transistor schematics for simple CMOS operational amplifiers from performance specifications and process parameters, and demonstrates the workability of the approac ...

9 A Forth-based hybrid neuron for neural nets

Paul Frenger
March 1991 **Proceedings of the second and third annual workshops on Forth**

Full text available: pdf(463.78 KB) Additional Information: full citation, references, citings, index terms

10 Systematic Design for Power Minimization of Pipelined Analog-to-Digital Converters
Reza Lotfi, Mohammad Taherzadeh-Sani, M. Yaser Azizi, Omid Shoaei
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(161.60 KB) Additional Information: full citation, abstract, index terms

In this paper a general method to design a pipelined ADC withminimum power consumption is presented. By expressing the totalpower consumption and the total input-referred noise of theconverter as functions of the capacitor values and the resolutions ofthe converter stages, an optimization algorithm is employed tocalculate the optimum values of these parameters, which lead tominimum power consumption while a specific noise requirement issatisfied. To determine the bias current values of operation ...

11 Behavioral synthesis of analog systems using two-layered design space exploration
Alex Doboli, Adrian Nunez-Aldana, Nagu Dhanwada, Sree Ganesan, Ranga Vemuri
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(165.35 KB) Additional Information: full citation, references, citings, index terms

12 Analog design space exploration: Architectural selection of A/D converters
Martin Vogels, Georges Gielen
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(139.39 KB) Additional Information: full citation, abstract, references, index terms

A method for the architectural selection of analog to digital (A/D) converters based on a generic figure of merit is described. First a figure of merit for the power consumption is introduced. This figure of merit includes both target specifications and technology data and has five generic parameters. The values of these generic parameters can be estimated by analyzing the different converter structures or by means of a fitting procedure using data from published designs. It is shown that the ge ...

Keywords: A/D conversion, power estimation

13 VLSI circuits: 40 MHz 0.25 um CMOS embedded 1T bit-line decoupled DRAM FIFO for mixed-signal applications
Michael I. Fuller, James P. Mabry, John A. Hossack, Travis N. Blalock
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**

Full text available: pdf(252.55 KB) Additional Information: full citation, abstract, references, index terms

An embedded 40 MHz FIFO buffer for use in mixed-signal information processing applications is presented. The buffer design uses a 1T DRAM topology for its unit memory cell component, a sense amplifier, and two circular shift registers for implementing refresh and read-write pointers. The sense amplifier uses bit-line decoupling to improve readout performance. Our particular application requires the storage of 800 samples of a received ultrasound signal that pass through 48 channels consisting of ...

Keywords: CMOS, DRAM, FIFO, embedded memory, ultrasound

14 An arbitrary chaos generator core curcuit using PWM/PPM signals
Kenichi Murakoshi, Takashi Morie, Makoto Nagata, Atsushi Iwata
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
Full text available: pdf(144.45 KB) Additional Information: full citation, references

15 Analog design: A 0.8 µm CMOS switched-capacitor video filter
Antonio Petraglia, Jorge Morales Cañive, Mariane Rembold Petraglia
September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**
Full text available: pdf(370.63 KB) Additional Information: full citation, abstract, references, index terms

The very low sensitivity properties of switched-capacitor filtering structures implemented as a parallel connection of two allpass sections has already been demonstrated theoretically and verified by computer simulation. This paper describes the design of a fifth-order lowpass elliptic filter using this technique, to satisfy specifications commonly used in video frequency applications. Operating with a sampling frequency of 16 MHz, the IC prototype was implemented in a standard double-poly CMOS ...

Keywords: allpass circuits, analog integrated circuits, filters, switched-capacitor filters, testing

16 Design and implementation of a field programmable analogue array
Adrian Bratt, Ian Macbeth
February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**
Full text available: pdf(139.04 KB) Additional Information: full citation, references, citings, index terms

17 Enhanced prediction of energy losses during adiabatic charging
A. Schlaffer, J. A. Nossek
August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**
Full text available: pdf(370.56 KB) Additional Information: full citation, references

18 Challenges in integrated CMOS transceivers for short distance wireless
Khurram Muhammad, Robert B. Straszewski, Poras T. Balsara
March 2001 **Proceedings of the 11th Great Lakes symposium on VLSI**
Full text available: pdf(797.97 KB) Additional Information: full citation, references, index terms

19 High-Level Synthesis of Analog Sensor Interface Front-Ends
S. Donnay, G. Gielen, W. Sansen, W. Kruiskamp, D. Leenaerts, W. Van Bokhoven
March 1997 **Proceedings of the 1997 European conference on Design and Test**
Full text available: pdf(592.46 KB) Publisher Site Additional Information: full citation, abstract

In this paper we compare three different methodologies for analog high-level synthesis.

Two optimization-based methods-one with simulations in the loop, the other with equations-and a library-based approach are discussed and illustrated with experimental results. The comparison is made by means of a real life design example-a radiation detector interface ASIC-although the methodologies presented in this paper, are generally applicable.

Keywords: sensors, analog high-level synthesis, analog sensor interface front-ends, optimization-based methods, library-based approach, radiation detector interface ASIC

20 A 3-pin 1.5 V 550 mW 176 x 144 self-clocked CMOS active pixel image sensor

Kwang-Bo Cho, Alexander Krymski, Eric Fossum

August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

Full text available: pdf(350.69 KB) Additional Information: full citation, references, index terms

Keywords: CMOS, active pixel sensor, image sensor, low-power, low-voltage, self-clocked

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